

REMARKS

Upon entry of this First Response, claims 1-18 and 30-38 remain pending in this application. Claims 1, 7, 13, 30, 31, and 33-37 are directly amended herein, and claims 27-29 are cancelled without prejudice or disclaimer via the amendments set forth herein.

It is believed that the foregoing amendments add no new matter to the present application. Examination, consideration, and allowance of the application and all presently pending claims are respectfully requested.

Response to Claim Objections

The outstanding Office Action indicates that claims 33-37 are objected to for various informalities. Claims 33-37 have been amended to correct such informalities, and Applicant respectfully requests that the claim objections corresponding to claims 33-37 be withdrawn.

Response to §112 Rejections

The outstanding Office Action indicates that claims 28 and 29 are rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the Office Action asserts that the limitation "the component" in line 1 of claim 28 lacks an antecedence basis because it does not define or is not understandable which component in claim 27 is an array.

However, Applicant has cancelled claims 27-29 via amendments made directly herein. Therefore, the 35 U.S.C. §112 rejection is now moot.

Response to §102 Rejections

A proper rejection of a claim under 35 U.S.C. §102 requires that a single prior art reference disclose each element of the claim. See, e.g., *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303, 313 (Fed. Cir. 1983).

Claim 1

Claim 1 is rejected under 35 U.S.C. 102(a) as being anticipated by *Taborn, et al.* Claim 1 reads as follows:

1. An exponent computation apparatus for performing overflow and underflow comparisons while minimizing overflow/underflow comparison circuitry, said apparatus comprising:
overflow/underflow possible check circuitry, said overflow/underflow possible check circuitry configured to determine if a mathematical operation involving a first exponent signal and a second exponent signal creates a potential overflow condition, *wherein said overflow/underflow possible check circuitry is configured to generate a underflow/overflow signal indicating if said overflow condition is a possibility and generate an exponent selection signal, and wherein said exponent selection signal is indicative of said first exponent signal if said first exponent signal is greater than said second exponent signal and is indicative of said second exponent signal if said second exponent signal is greater than said first exponent signal; and*
exponent compare circuitry configured to compute an actual overflow/underflow condition for said first or second exponent signal based upon said exponent selection signal, said exponent compare circuitry configured to compute an actual overflow condition if said underflow/overflow signal indicates overflow is possible, said exponent compare circuitry configured to compute an actual underflow condition if said underflow/overflow signal does not indicate overflow is possible.
(Emphasis added).

Applicant respectfully asserts that the cited art fails to disclose at least the features of amended claim 1 highlighted hereinabove. Accordingly, the 35 U.S.C. §102 rejection of claim 1 should be withdrawn.

In particular, it is asserted in the Office Action that *Taborn et al.* discloses: “overflow/underflow possible check circuitry configured to generate a signal indicating if overflow condition is a possibility” and “exponent compare circuitry (78-79)...configured to compute an actual overflow/underflow condition (78-79)...if signal indicates overflow is possible (79 with output of 80 as 72 enable)...and underflow condition if signal does not indicate overflow is possible (78 with output of 72 enable).” See Office Action, page 3-4.

However, Applicant asserts that *Taborn et al.* fails to disclose that the alleged “overflow/underflow possible check circuitry” is “configured to generate a signal indicating if said overflow condition is a possibility and generate an exponent selection signal indicative of said first exponent signal if said first exponent signal is greater than said second exponent signal or generate said exponent selection signal indicative of said second exponent signal if said second exponent signal is greater than said first exponent signal,” as recited in claim 1. *Taborn et al.* fail to disclose that the alleged “exponent compare circuitry” is configured to “compute an actual overflow/underflow condition for said first or second exponent signal based upon said exponent selection signal,” as recited by claim 1.

In light of the foregoing, Applicant respectfully requests that the 35 U.S.C. §102 rejection of claim 1 be withdrawn.

Claims 2-6, 30, 31, 38, and 39

Claims 2-6, 30, 31, and 38 presently stand rejected in the Office Action under 35 U.S.C. §102 as allegedly anticipated by *Taborn et al.*, and claim 39 is newly added. Applicant submits that the pending dependent claims 2-6, 30, 31, 38, and 39 contain all features of their respective independent claim 1. Since claim 1 should be allowed, as argued hereinabove, pending

dependent claims 2-6, 30, 31, 38, and 39 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 7

Claim 7 is rejected under 35 U.S.C. §102 as allegedly anticipated by *Taborn, et al.*

Claim 7 reads as follows:

7. A method for performing overflow and underflow comparisons with exponent comparison circuitry, comprising the steps of:

- determining if a mathematical operation creates a potential overflow condition;
- generating an underflow/overflow signal indicating if said potential overflow condition exists;
- determining which of said first and second exponent signals is greater;
- generating, based on said determining step, an exponent selection signal indicative of said first exponent signal if said first exponent signal is greater than said second exponent signal and indicative of said second exponent signal if said second exponent signal is greater than said first exponent signal;*
- computing an actual overflow condition for said first or second exponent signal based upon said exponent selection signal* with said exponent comparison circuitry if said underflow/overflow signal indicates that a potential overflow condition exists; and
- computing an actual underflow condition for said first or second exponent signal based upon said exponent selection signal* with said exponent comparison circuitry if said underflow/overflow signal indicates said potential overflow condition does not exist. (Emphasis added).

For at least those reasons argued hereinabove with respect to pending claim 1, Applicant submits that *Taborn et al.* fails to disclose at least the features of claim 7 highlighted hereinabove. Therefore, Applicant respectfully requests that the 35 U.S.C. §102 rejection of claim 7 be withdrawn.

Claims 8-12

Claims 8-12 presently stand rejected in the Office Action under 35 U.S.C. §102 as allegedly anticipated by *Taborn et al.* Applicant submits that the pending dependent claims 8-12 contain all features of their respective independent claim 7. Since claim 7 should be allowed, as argued hereinabove, pending dependent claims 8-12 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 13

Claim 13 is rejected under 35 U.S.C. §102 as being anticipated by *Taborn, et al.* Claim 13 reads as follows:

13. An exponent computation apparatus for performing overflow and underflow comparisons while minimizing overflow/underflow comparison circuitry, the apparatus comprising:
means for determining if a mathematical operation creates a potential overflow condition;
means for generating an underflow/overflow signal indicating if said potential overflow condition exists;
means for generating an exponent selection signal, said exponent selection signal indicative of said first exponent signal if said first exponent signal is greater than said second exponent signal and indicative of said second exponent signal if said second exponent signal is greater than said first exponent signal; and
means for computing an actual overflow condition for said first or second exponent signal based upon said exponent selection signal if said underflow/overflow signal indicates said potential overflow condition exists and an actual underflow condition for said first or second exponent signal based upon said exponent selection signal if said signal indicates said potential overflow condition does not exist. (Emphasis added).

For at least those reasons argued hereinabove with respect to pending claim 1, Applicant submits that *Taborn et al.* fails to disclose at least the features of claim 13 highlighted hereinabove. Therefore, Applicant respectfully requests that the 35 U.S.C. §102 rejection of claim 7 be withdrawn.

Claims 14-18

Claims 14-18 presently stand rejected in the Office Action under 35 U.S.C. §103 as allegedly being unpatentable over *Taborn et al.* Applicant submits that the pending dependent claims 14-18 contain all features of their respective independent claim 13. Since claim 13 should be allowed, as argued hereinabove, pending dependent claims 14-18 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

Claim 32

Claim 32 is rejected under 35 U.S.C. §102 as being anticipated by *Taborn, et al.* Claim 32 reads as follows:

32. A method for performing overflow and underflow comparisons with exponent comparison circuitry, comprising the steps of:
selecting an exponent precision underflow/overflow constant from a plurality of exponent underflow/overflow constants;
generating a sum signal and a carry signal from one of said plurality of exponent underflow/overflow constants, a pre-normalized exponent signal and a normalization shift amount signal;
computing an underflow/overflow result from said sum signal and said carry signal; and
transmitting an underflow/overflow condition based upon said underflow/overflow result and an exponent adjust amount signal. (Emphasis added).

Applicant submits that *Taborn et al.* fails to disclose at least each of the features of claim 32 highlighted hereinabove. Accordingly, the 35 U.S.C. §102 rejection of claim 32 is improper.

In particular, it is asserted in the Office Action states that *Taborn et al.* discloses generating an “output value of 39 or the final answer” from the “output of 10,” where reference numeral 10 refers to circuitry that produces an underflow or overflow error signal. See, *Taborn*

et al., column 7, lines 39-47. The error signal produced indicates “whether underflow or overflow error has occurred.” See, *Taborn et al.*, column 7, lines 41-42.

However, it does not appear that such error signal is produced by “generating a sum signal and a carry signal from one of said plurality of exponent underflow/overflow constants, a pre-normalized exponent signal and a normalization shift amount signal” and “computing an underflow/overflow result from said sum signal and said carry signal,” as recited in claim 32.

In light of the foregoing, it does not appear that *Taborn et al.* discloses each feature recited in claim 32. Accordingly, Applicant respectfully requests that the 35 U.S.C. §102 rejection of claim 32 be withdrawn.

Claims 33-37

Claims 33-37 are rejected under 35 U.S.C. §102 as being anticipated by *Taborn, et al.* Applicant submits that the pending dependent claims 33-37 contain all features of their respective independent claim 32. Since claim 32 should be allowed, as argued hereinabove, pending dependent claims 33-37 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

CONCLUSION

Applicant respectfully requests that all outstanding objections and rejections be withdrawn and that this application and all presently pending claims be allowed to issue. If the Examiner has any questions or comments regarding Applicant's response, the Examiner is encouraged to telephone Applicant's undersigned counsel.

Respectfully submitted ,

**THOMAS, KAYDEN, HORSTEMEYER
& RISLEY, L.L.P.**

By: 

Ann I. Dennen
Reg. No. 44,651
(256) 704-3900 Ext. 101

Intellectual Property Administration
P.O. Box 272400
Fort Collins, Colorado 80527-2400